

## **AMENDMENTS TO THE CLAIMS**

**1. (Previously Presented)** A semiconductor device comprising:  
a semiconductor substrate having a pattern forming region and a pattern non-forming region;  
a wiring pattern formed on said pattern forming region;  
a plurality of dummy patterns formed on said pattern non-forming region, said plurality of dummy patterns being formed within a plurality of dummy areas, and each of the plurality of dummy areas having a same shape; and  
an insulating film formed on said wiring pattern and said plurality of dummy patterns;  
wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing;  
wherein each of said dummy patterns has a plurality of parallel line patterns, each of said line patterns of said plurality of line patterns being spaced apart from each other by an area filled by the deposition of said insulating film; and  
wherein a distance between each of said line patterns of said plurality of line patterns is less than 72  $\mu\text{m}$ .

**2-4. (Cancelled)**

**5. (Previously Presented)** A semiconductor device according to claim 1, wherein the dummy areas each have a square shape.

**6. (Previously Presented)** A semiconductor device according to claim 1, wherein the dummy areas are arranged in lattice form.

**7. (Cancelled)**

**8. (Previously Presented)** A semiconductor device according to claim 1, wherein said plurality of dummy patterns are line patterns.

**9. (Previously Presented)** A semiconductor device comprising:  
a semiconductor substrate having a pattern area and a non-pattern area;  
a conductive pattern formed on said pattern area of said semiconductor substrate; and  
a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate, each of said plurality of dummy patterns having a same continuous rectangular outline shape as each other and being arranged in a matrix with predetermined spacing; and  
an insulating film formed on said conductive pattern and said plurality of dummy patterns;  
wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing;  
wherein each of said dummy patterns has only one square-shaped opening so that a pattern ratio of said semiconductor device is reduced; and  
wherein a width of the opening of each of said dummy patterns is less than 72  $\mu\text{m}$ .

**10. (Previously Presented)** A semiconductor device according to claim 9, wherein each of said plurality of dummy patterns has a square outline.

**11-13. (Cancelled)**

**14. (Previously Presented)** A semiconductor device comprising:  
a semiconductor substrate having a pattern area and a non-pattern area;  
a conductor pattern formed on said pattern area of said semiconductor substrate;  
a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate;  
an insulating film formed on said conductive pattern and said plurality of dummy patterns;  
wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing;

wherein each of said plurality of dummy patterns are formed in a plurality of dummy areas, each of said plurality of dummy areas having a same shape, and each of said plurality of dummy patterns being arranged in a matrix with predetermined spacing;

wherein each of said dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of said semiconductor device is reduced; and

wherein each of said dummy patterns includes an opening at the space portion, the opening having a shape of a letter or a number, each opening of said dummy patterns having a width less than 72  $\mu\text{m}$ .

**15. (Previously Presented)** A semiconductor device according to claim 14, wherein each of said dummy patterns has a rectangular outline.

**16-17. (Cancelled)**

**18. (Previously Presented)** A semiconductor device according to claim 15, wherein the opening has a shape of a plurality of letters.

**19-20. (Cancelled)**

**21. (Previously Presented)** A semiconductor device according to claim 1, wherein said line patterns are arranged in a same direction.

**22. (New)** A semiconductor device according to claim 14, wherein the openings of the dummy patterns each have a shape different from one another.

**23. (New)** A method of manufacturing the semiconductor device of claim 1, the method comprising:

forming the wiring pattern and the dummy patterns above the semiconductor substrate;  
forming the insulating film on the wiring pattern and the dummy patterns by chemical

vapor deposition, an area between line patterns being filled by the insulating film; and  
smoothing the insulating film by chemical mechanical polishing.

**24. (New)** A method of manufacturing the semiconductor device of claim 9, the method comprising:

forming the conductive pattern and the dummy patterns above the semiconductor substrate;

forming the insulating film on the conductive pattern and the dummy patterns by chemical vapor deposition, the opening of each dummy pattern being filled by the insulating film; and

smoothing the insulating film by chemical mechanical polishing.

**25. (New)** A method of manufacturing the semiconductor device of claim 14, the method comprising:

forming the conductor pattern and the dummy patterns above the semiconductor substrate;

forming the insulating film on the conductor pattern and the dummy patterns by chemical vapor deposition, the opening of each dummy pattern being filled by the insulating film; and

smoothing the insulating film by chemical mechanical polishing.

**26. (New)** The method according to claim 23, wherein the insulating film is Boro Phospho Silicate Glass (BPSG) oxide film.

**27. (New)** The method according to claim 23, wherein the insulating film is High Density Plasma-Chemical Vapor Deposition (HDP-CVD) oxide film.

**28. (New)** The method according to claim 24, wherein the insulating film is Boro Phospho Silicate Glass (BPSG) oxide film.

**29. (New)** The method according to claim 24, wherein the insulating film is High Density Plasma-Chemical Vapor Deposition (HDP-CVD) oxide film.

**30. (New)** The method according to claim 25, wherein the insulating film is Boro Phospho Silicate Glass (BPSG) oxide film.

**31. (New)** The method according to claim 25, wherein the insulating film is High Density Plasma-Chemical Vapor Deposition (HDP-CVD) oxide film.